IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the Application of:		)
		)
MPR		) **Electronically Filed**
		)
U.S. Serial No.:	10/606,216	)
		)
Filed:	6/25/2003	)
		)
Examiner:	Wong	)
		)
Group Art Unit:	2621	)
		)
Confirmation No.	3721	)

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This appeal is an appeal of the Final Office Action of 7/25/08. A Notice of Appeal was filed on 10/21/2008, concurrently with a Pre-Appeal Brief Request for Review and correspondence providing the reasons that the Pre-Appeal Brief Request for Review was requested.

No Pre-Appeal Conference or Pre-Appeal Decision has yet been made. Since the deadline for filing the Appeal Brief is the *later* of two months from the filing of the Notice of Appeal and an adverse Pre-Appeal Decision, it is respectfully submitted that this appeal brief is timely and not fees for extensions are required.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore, as set forth in the Assignment filed with the present application and recorded on February 25, 2009 at Reel 014002 Frame 0814.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being obvious from U.S. Patent 5,903,311 to Ozcelik ("Ozcelik") in view of U.S. Patent 6,130,963 to Uz ("Uz").

Claim 6 was rejected under 35 U.S.C. 103(a) as being obvious from U.S. Patent 5,903,311 to Ozcelik in view of Uz and further in view of U.S. Patent 6,130,963 to Luna ("Luna").

Claims 7-12 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz.

Claims 13 and 14 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz and in further view of Luna.

Claim 15 was rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz.

Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz and in further view of Luna.

Claim 18 was rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

Clain 19 was rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik.

Claim 20 was rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

Claim 21 was rejected under 35 U.S.C. 103(a) as being anticipated by Ozcelik.

Claims 22 and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

The rejections of claims 1, 2, 7, 8, 13, 14, and 18 are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a method for displaying progressive frames, said method comprising: displaying a first portion of a progressive frame; and writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

Several embodiments of claim 1 are described in the specification, for example:

(1) Claim 1 is described in the specification, for example, the specification, Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Displaying progressive frames comprises displaying a first portion (Figure 5A, **105a**) of a progressive frame (0052, "After decoder 245 decodes portion **105a** and writes portion **105a** into the top region of **270(1)(c)** [Figure 3], the display engine displays portion **105a.)**".

The specification also describes writing a second portion of the progressive frame (for example, portion **105b**) while displaying the first portion of the progressive frame (portion **105a**) (0053 - "While the display engine 250 displays portion **105a**, the decoder can decode portion **105b** and write portion **105b** to bottom region **270(2)(c).**").

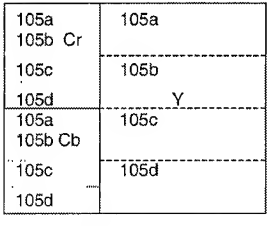


FIGURE 5A

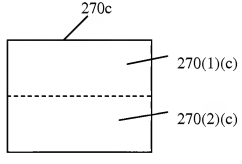


FIGURE 3
(Portion, Formalized)

(2) **(First Portion 105b, Second Portion 105c)** Another embodiment of claim 1 is also described in the

specification. The specification Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Additionally, the specification discloses displaying progressive frames comprises displaying a first portion (Figure 5A, **105b**) of a progressive frame (0053, "the display engine 250 displays portion **105b**").

Additionally, the specification describes writing a second portion of the progressive frame (for example, portion **105c**) while displaying the first portion of the progressive frame (portion **105b**) (0053 - "While the display engine 250 displays portion **105b**, the decoder can decode portion **105c** and overwrite portion **105a** in region **270(1)(c)**.").

(3) **(First Portion 105c, Second Portion 105d)** Another embodiment of claim 1 is also described in the specification. The specification Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Additionally, the specification discloses displaying progressive frames comprises displaying a first portion (Figure 5A, **105c**) of a progressive frame (0052, "After decoder 245 decodes portion **105c** and writes portion **105c** into the top region of **270(1)(c)** [Figure 3], the display engine displays portion **105c**.)".

Additionally, the specification describes writing a second portion of the progressive frame (for example, portion **105d**) while displaying the first portion of the progressive frame (portion **105c**) (0053 - "While the display

engine 250 displays portion **105c**, the decoder can decode portion **105d** and overwrite portion **105b** in region **270(2)(c).**").

Claim 2 is directed to the method of claim 1, wherein writing the second portion of the progressive frame further comprises overwriting a third portion of the progressive frame with the second portion of the progressive frame.

The specification describes writing the second portion of the frame 105c/105d further comprises overwriting a third portion 105a/105b of the frame with the second portion of the frame (if claim 1 is embodiment 2, "While the display engine 250 displays portion 105b from region 270(2)(c), the decoder 245 can decode portion 105c and overwrite portion 105a in region 270(1)c)" – **first portion 105b**, **second portion 105c**, **third portion 105a;** if claim 1 is embodiment 3, 0053 – "While the display engine 250 displays portion 105c, the decoder can decode portion 105d and overwrite portion 105b in region 270(1)(2)" – **first portion 105c**, **second portion 105d**, **third portion 105b**).

Claim 7 is directed to a circuit for displaying progressive frames. The circuit comprises a memory, a display engine, and a controller. The memory stores a first portion of a progressive frame. The display engine displays the first portion of the progressive frame. The controller writes a second portion of the progressive frame in the memory, while the display engine displays the first portion.

Several Embodiments of claim 7 are described in the specification:

(1) Claim 7 is described in the specification, for example, the specification, for example, Figure 2 and

Figure 5A, 0049-0054 describe a circuit displaying progressive frames (Figure 2, generally, 0049 “There is illustrated a block diagram of an exemplary decoded progressive frame 105.” See also, Figure 5A). The circuit comprises a memory (Figure 2, frame buffers 270), a display engine (Figure 2, Display Engine 350) and a controller (MPEG Video Decoder 345).

The memory (Figure 3, 270c) stores a first portion of a progressive frame (0052 “After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c)…”).

The display engine displays progressive frames comprises displaying a first portion (Figure 5A, 105a) of a progressive frame (0052, “After decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c) [Figure 3], the display engine displays portion 105a.)”.

The controller writes a second portion of the progressive frame (for example, portion 105b) while the display engine displays the first portion of the progressive frame (portion 105a) (“While the display engine 250 displays portion 105a, the decoder can decoded portion 105b and write portion 105b to bottom region 270(2)(c).”).

(2) First Portion 105b, Second Portion 105c

(3) First Portion 105c, Second Portion 105d

Claim 8 is directed to the circuit of claim 7 wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame.

The specification describes the controller overwrites overwrites a third portion 105a/105b of the progressive frame with the second portion 105(c)/105d of the

progressive frame (if claim 7 is embodiment 2, "While the display engine 250 displays portion 105b from region 270(2)(c), the decoder 245 can decode portion 105c and overwrite portion 105a in region 270(1)c)" - **first portion 105b, second portion 105c, third portion 105a;** if claim 7 is embodiment 3, 0053 - "While the display engine 250 displays portion 105c, the decoder can decode portion 105d and overwrite portion 105b in region 270(1)(2)" - **first portion 105c, second portion 105d, third portion 105b**).

Claim 13 is directed to the circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.

Claim 13 is directed to the circuit of claim 12 (first prediction buffer, 270a, second prediction frame buffer 270b, delta frame buffer 270c), wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution [0044].

Claim 14 is directed to the circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution.

Claim 14 is directed to the circuit, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive

frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution [0042].

Claim 15 is directed to an integrated circuit. The integrated circuit comprises a first prediction buffer, a second prediction buffer, and a delta frame buffer. The first prediction frame buffer stores a first frame. The second prediction frame buffer stores a second frame. The delta frame buffer stores a portion of a third frame.

Claim 15 is described in the specification, for example, specification 0070 and Figure 3. The specification describes an integrated circuit [0070]. The integrated circuit comprises a first prediction buffer (Figure 3, 270a), a second prediction buffer (270b), and a delta frame buffer (270c). The first prediction frame buffer stores a first frame (0041). The second prediction frame buffer stores a second frame (0041). The delta frame buffer stores a portion of a third frame (0042).

Claim 18 is directed to a circuit for displaying interlaced frames. The circuit comprises a memory, a display engine, and a controller. The memory stores a first portion of a field. The display engine displays the first portion of the field. The controller writes a second portion of the field in the memory, while the display engine displays the first portion of the field.

Claim 18 is described in the specification, for example, Figure 2 describes a circuit for displaying interlaced frames (Figure 5B, 105(0), 105(1)).

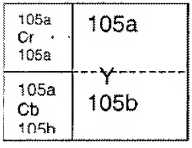


FIGURE 5A

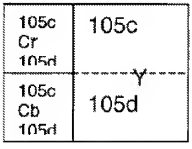


FIGURE 5B

The memory stores a first portion of a field (0057 - "In the case of an interlaced frame, the first portion can comprise the first n/64 rows of macroblocks 108 in the top field 105(0))", in connection with 0052 "After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c)…").

The display engine displays the first portion of the field (0057 - "In the case of an interlaced frame, the first portion can comprise the first n/64 rows of macroblocks 108 in the top field" in connection with 0052, "After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c), the display engine 250 displays portion 105a").

The controller writes a second portion of the field in the memory, while the display engine displays the first portion of the field (0057 - "The second portion 105b can comprises the remaining macroblocks 108 of the top field 105(0)" in connection with 0053, "While the display engine 250 displays portion 105a, the decoder can decode portion 105b and write portion 105b to bottom region 270(2)(c).").

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 2, 7, and 8 are obvious from Ozcelik in view of Uz.

Whether claims 13 and 14 are obvious from Ozcelik in view of Uz, and further in view of Luna.

Whether claim 18 is anticipated by Ozcelik.

VII. ARGUMENT: THE REJECTION TO CLAIMS 1 AND 7 SHOULD BE REVERSED BECAUSE OZCELIK AND UZ CANNOT BE COMBINED TO RESULT IN ALL OF THE LIMITATIONS OF CLAIMS 1 AND 7

Claim 1 is reproduced below:

> 1. A method for displaying progressive frames, said method comprising:
> displaying a first portion of a progressive frame; and
> writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

Claim 7 is reproduced below:

> A circuit for displaying progressive frames, said circuit comprising:
> a memory for storing a first portion of a progressive frame;
> a display engine for displaying the first portion of the progressive frame; and
> a controller for writing a second portion of the progressive frame in the memory, while the display engine displays the first portion.

A. Rejection of Claim 1

The rejection to claim 1 in the final office action (FOA) of 7/25/08 is summarized below for each claim element.

A method for displaying progressive frames, said method comprising:	Ozcelik discloses a method for displaying frames, said method comprising: FOA at 5.
displaying a first portion of a progressive frame; and	displaying a first portion of a frame (col. 12, ln 19-34; Ozcelik discloses that the first portion, ie. top field, is displayed for a frame); FOA at 5.
writing a second portion of the progressive frame while displaying the first portion of the progressive frame.	Ozcelik discloses the second portion, ie. bottom field, of the frame is written or buffered for storage while the first portion, ie., top field, is displayed. FOA at 5.

Examiner concedes that Ozcelik does not specifically disclose progressive frames, while Uz teaches progressive frames. Examiner concludes that it would be obvious to combine the teachings of Ozcelik and Uz for efficiently displaying high quality progressive video images while reducing noise.

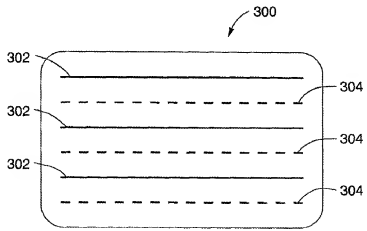
Regarding claim 7, Examiner also states that "Ozcelik discloses the second portion, ie. bottom field, of the frame is written or buffered for storage while the first portion, ie., top field, is displayed" and relies on the progressive frames taught by Uz.

B. THE INTERLACED FRAMES OF OZCELICK CANNOT BE MODIFIED WITH THE PROGRESSIVE FRAMES OF UZ AND STILL MEET THE LIMITATIONS OF CLAIMS 1 AND 7

Appellant respectfully submits that the above conclusion is in error because modifying the interlaced frames in Ozcelik with the progressive frames of Uz, would either inoperable to perform the recited limitations.

Video frames are either interlaced or progressive. Frames are two-dimensional grids of pixels. Interlaced frames are divided into even numbered lines and odd numbered lines. Ozcelik, Figure 3 is an exemplary illustration of an interlaced frame. The even numbered lines are captured and displayed at one time instant followed by the odd numbered lines at another time instant, or vice versa. The even numbered lines in interlaced frames are known as the top field, while the odd numbered lines are known as the bottom field. Progressive frames on the other hand, are displayed sequentially, from top to bottom. Progressive frames are associated with one time period.

Ozcelik, Figure 3 illustrates an exemplary interlaced frame:



Ozcelik, Figure 3

Rows 302 are the top field, while rows 304 are the bottom field. It is also noted that top fields and bottom fields are encoded as separate units in the MPEG-2 standard. Progressive frames, on the other hand, are not.

If the Ozcelik were modified to use the *progressive images* of Uz, it would not be possible for "*bottom field* of the frame is written or buffered for storage while the first portion, ie. *top field*, is displayed", since progressive frames do not have top fields and bottom fields. That which Examiner relies on as the first portion and second portion of the frame, the top field, and bottom field, would no longer exist if Ozcelik used progressive frames.

VIII. ARGUMENT: THE REJECTION TO CLAIMS 2 AND 8 SHOULD BE REVERSED BECAUSE NEITHER OZCELIK OR UZ TEACH "OVERWRITING THE THIRD PORTION OF THE … FRAME WITH THE SECOND PORTION"

Claims 2 and 8 are reproduced below:

> 2. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:
> overwriting a third portion of the progressive frame with the second portion of the progressive frame.

> 8. The circuit of claim 7, wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame in the memory.

Examiner has indicated that:

> Ozcelik discloses overwriting (col. 12, ln 19-34, note data can be overwritten… Ozcelik does not

> specifically disclose the use of a third and fourth portions of a frame. However, Ozcelik teaches the use of a subpicture decoder (col. 7, ln 45-64, Ozcelik discloses that element 420 of figure 4 is a subpicture decoder used to decode multiple subpicture portions of image data within a frame for decoding images utilized in DVD applications, thus permitting use of first, second, third, fourth, fifth or more sections for storing multiple sections or portions of image data.

FOA at 6.

For the sake of argument, even if the following is true (which Appellant does not admit):

(1) Ozcelik teaches overwriting; and

(2) Ozcelik teaches use of a first, second, third, fourth, fifth or more portions of a frame

The rejection is in error because it fails to establish that either Ozcelik, alone, or in combination with Uz teaches, "overwriting a third portion of the progressive frame with the second portion of the progressive frame". Appellant respectfully submits that merely teaching overwriting and use of first, second, and third portions of the frame, does not teach overwriting the third portion with the second portion.

Moreover, Examiner has indicated that Ozcelik permits "use of first, second, third, fourth, fifth or more sections for **storing** multiple sections or portions of image data." It would follow that if there were multiple sections for storing, Ozcelik would not **overwrite** the one of the "first, second, third, fourth, fifth or more portions of a frame" with another of the first, second, third, fourth, fifth or more portions of a frame.

Accordingly, Assignee respectfully submits that the rejection to claims 2 and 8 should be REVERSED because the combination of Ozcelik and Uz does not teach all of the limitations of claims 2 and 8.

IX. ARGUMENT: THE REJECTIONS TO CLAIMS 13 AND 14 SHOULD BE REVERSED THE PROPOSED COMBINATION OF OZCELIK AND UZ COULD NOT BE COMBINED WITH LUNA TO TEACH THE LIMITATIONS OF CLAIMS 13 AND 14.

Claims 13 and 14 are reproduced below:

> 13. The circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.
>
> 14. The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution.

Examiner has indicated that Ozcelik discloses "frames are stored in buffers no more than the seize of 4 megabytes (col. 4, ln. 55-57, note 3X or approximately 3 megabyte is needed for buffering the frame data". Office Action at 11. Examiner has also indicated that "Ozcelik and Uz do not specifically discloses the use of high definition television frames with at least" "1280x720 resolution", "1920x1080". OA at 11; 12. "However, Luna teaches the use

of high definition television frames with at least" "1280x720 resolution" "1920x1080". OA at 12. "It would have been obvious to … use well known term of 'high definition television' … for viewing clear images for viewing in high definition monitors and televisions so as to enjoy enhanced quality images when watching movies and televised programming." OA at 12.

Assignee respectfully submits that the foregoing is in error because if Ozcelik and Uz were modified to use high definition television, it would no longer be the case that "3 megabytes is needed for buffering the frame data". It is noted that Ozcelik uses standard NTSC size frames of 720x480 pixels. See Col. 4, Line 41. Clearly when higher resolution frames are used, e.g., 1280x720 (almost three time more pixels), or 1920x1080 (six times more pixels), more memory is required.

Accordingly, Appellant respectfully requests the rejections to claims 13 and 14 be REVERSED.

X. ARGUMENT: THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE OZCELIK DOES NOT TEACH ALL OF THE LIMITATIONS

Claim 18 is reproduced below:

> A circuit for displaying interlaced frames, said circuit comprising:
> a memory for storing a first portion of a field;
> a display engine for displaying the first portion of the field; and
> a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field.

Claim 18 was rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik. Examiner indicated that Ozcelik disclosed "a controller for writing a second portion *of the field* in the memory while the display engine displays the first portion of the field (col. 12, ln 19-41; Ozcelik discloses the second portion, ie. Bottom field, *of the frame* is written or buffered for storage while the first portion, ie., top field, is displayed)."

Appellant respectfully submits that the top field and bottom field cannot be the "first portion of the field" and the "second portion of the field", because the top field and the bottom field are different fields. Both instances of "the field" take antecedent basis from the earlier recited "a field". Thus, the first portion of the field and the second portion of the field must be portions of the same field.

Accordingly, Appellant respectfully submits that the rejection to claim 18 is in error because Ozcelick does not teach "a controller for writing a second portion of *the* field in the memory, while the display engine displays the first portion of *the* field". Appellant respectfully requests that the rejection be REVERSED.

XI. CONCLUSION

For at least the foregoing reasons, the Board of Patent Appeals and Interferences is respectfully requested to REVERSE the rejections to claims 1, 2, 7, 8, 13, 14, and 18.

The Commissioner is hereby required to charge any overpayments or additional fees to Deposit Account No. 13-0017.

Dated: May 22, 2009

Respectfully submitted,

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CLAIMS APPENDIX

CLAIM LISTING

Please amend the claims as follows:

1. A method for displaying progressive frames, said method comprising:

displaying a first portion of a progressive frame; and

writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

2. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

overwriting a third portion of the progressive frame with the second portion of the progressive frame.

3. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

decoding the second portion of the progressive frame.

4. The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame;

overwriting the first portion of the progressive frame with a fourth portion of the progressive frame.

5. The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

overwriting the first portion of the progressive frame with a first portion of another progressive frame while displaying the second portion of the progressive frame.

6. The method of claim 1, wherein the progressive frame comprises a high definition television progressive frame.

7. A circuit for displaying progressive frames, said circuit comprising:

a memory for storing a first portion of a progressive frame;

a display engine for displaying the first portion of the progressive frame; and

a controller for writing a second portion of the progressive frame in the memory, while the display engine displays the first portion.

8. The circuit of claim 7, wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame in the memory.

9. The circuit of claim 7, wherein the controller decodes the second portion of the progressive frame.

10. The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a fourth portion of the progressive frame in the memory.

11. The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a first portion of another progressive frame while the display engine displays the second portion of the progressive frame.

12. The circuit of claim 7, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the progressive frame and the second portion of the progressive frame.

13. The circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.

14. The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise

high definition television progressive frames with at least 1920x1080 resolution.

15. An integrated circuit for storing decoded frames, said integrate circuit comprising:

a first prediction frame buffer for storing a first progressive frame;

a second prediction frame buffer for storing a second progressive frame; and

a delta frame buffer for storing a portion of a third progressive frame.

16. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 4 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the third progressive frame comprise high definition television frames with at least 1280x720 resolution.

17. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 8 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the third progressive frame comprise high definition television frames with at least 1920x1080 resolution.

18. A circuit for displaying interlaced frames, said circuit comprising:

a memory for storing a first portion of a field;

a display engine for displaying the first portion of the field; and

a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field.

19. The circuit of claim 18, wherein the controller overwrites a third portion of the field with the second portion of the field in the memory.

20. The circuit of claim 18, wherein the controller decodes the second portion of the field.

21. The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a fourth portion of the field in the memory.

22. The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a first portion of another field while the display engine displays the second portion of the field.

23. The circuit of claim 18, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the field and the second portion of the field.

EVIDENCE APPENDIX

There are no pages in this Appendix.

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.